Bi-Directional GaNFast™

CERTIFIED CARBON NEUTRAL company
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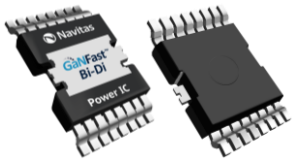
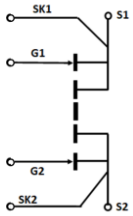
Top-Cooled TOLT-16L





Symbol

1. Features

- Bi-Directional 4-Quadrant GaN power switch:
  - V_{SS} 650V continuous / 800V transient
  - 80mΩ $R_{SS(ON)\_TYP\_25C}$ and 30A $I_{SS(CONT\_25C)}$
  - TOLT-16L thermally-enhanced, top-cooled
  - Zero reverse-recovery charge
  - Up to 2MHz operation
- *GaNFast*™ technology:
  - Integrated substrate clamp circuit between each source and the common substrate, optimizing switching performance in bi-directional current flow
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

- Solar Micro-inverter / ESS and Heric Inverter
- Bi-Directional ZVS Cyclo-converter topologies
- AC-AC Motor Drive and Matrix Converters
- Next-generation Bi-Directional topologies

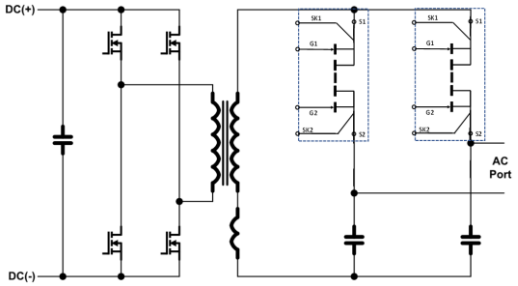
3. Description

NV6426 is an ***optimized*** bi-directional switch capable of blocking voltage in both directions. A monolithic, integrated substrate clamping circuit between each source and the common substrate automatically clamps source-to-substrate voltage. Navitas' unique substrate clamp technology allows optimized switching performance during 4-quadrant operation versus a ***floating substrate*** switch which can suffer 'back-gating effect'.

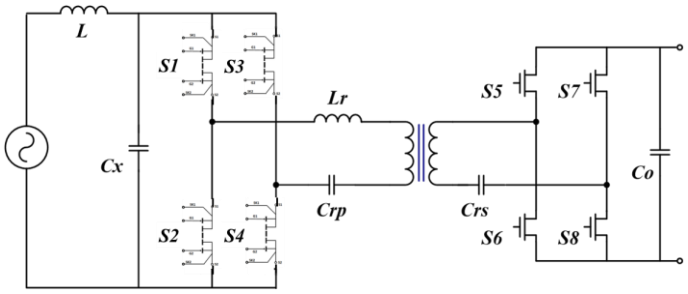
NV6426 also implements a thermally-enhanced top-cooled SMD with gull wing leads for superior board level temp cycling.

NV6426 is the ideal choice for topologies utilizing 4-quadrant switches to capture the benefits of bi-directional GaN for high-frequency, high-power-density, high-efficiency systems in solar, industrial, motor drive, and EV segments.

4. Typical Application Circuits



Cycloconverter



Ultra-High Power Density Onboard Charger

5. Table of Contents

6. Nomenclature

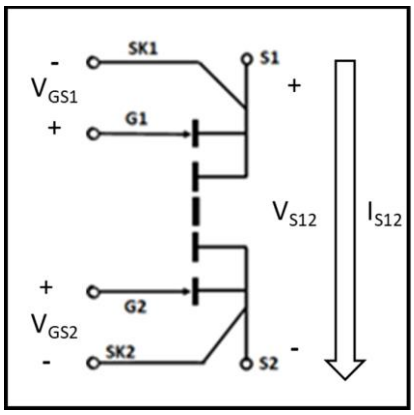


Fig. 1. V_{GS1}, V_{GS2}, V_{S12}, I_{S12} Definition (Note 1 – 3)

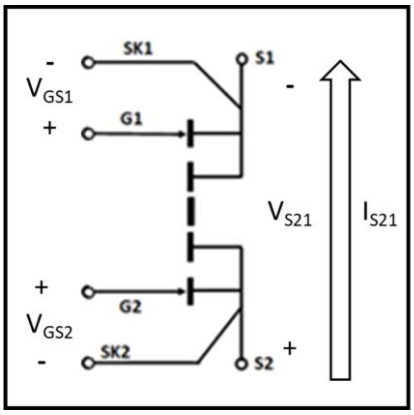


Fig. 2. V_{GS1}, V_{GS2}, V_{S21}, I_{S21} Definition (Note 1 – 3)

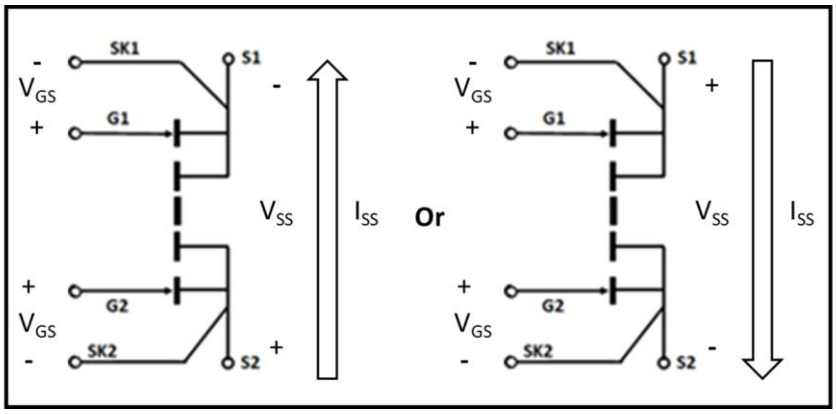


Fig. 3. V_{GS}, V_{SS}, I_{SS} Definition (Note 4 – 6)

(1) V_{GS1} implies that voltage is measured from gate_1 to source_1.
(2) V_{S12} implies that voltage is measured from source_1 to source_2.
(3) I_{S12} implies that current is flowing from source_1 to source_2.
(4) V_{GS} implies that $V_{GS} = V_{GS1} = V_{GS2}$.
(5) V_{SS} implies that the source-to-source voltage can be applied in either direction.
(6) I_{SS} implies that the source-to-source current can flow in either direction.
(7) The device is symmetric. All measurements listed with respect to gate_1 or source_1 are the same when measured with respect to gate_2 or source_2.

7. Absolute Maximum Ratings (Note 8) (with respect to source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{SS\_(CONT)}$	Continuous Source-to-Source Voltage	-650 to +650	V
$V_{SS\_(TRAN)}$	Transient Source-to-Source Voltage (Note 9)	-800 to +800	V
V_{GS}	Continuous Gate-to-Source Voltage	-10 to +7	V
$V_{GS\_(TRAN)}$	Transient Gate-to-Source Voltage	-20 to +10	V
$I_{SS\_(CONT)}$	Continuous Current (T_{CASE} = 25°C) Continuous Current (T_{CASE} = 100°C, T_{JUNC} = 150°C)	30 19	A
$I_{SS\_(PULSE)}$	Pulsed Current (10µs @ T_{JUNC} = 25°C) Pulsed Current (10µs @ T_{JUNC} = 150°C)	52 22	A
dV/dt	Source-to-Source Slew Rate	30	V/ns
T_{JUNC}	Operating Junction Temperature	-40 to +150	°C
T_{STOR}	Storage Temperature	-55 to +150	°C

(8) Absolute maximum ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(9) $V_{SS\_(TRAN)}$ allows for surge ratings during ***non-repetitive*** events that are < 100µs.

8. Recommended Operating Conditions (Note 10)

Symbol	Parameter	Min	Typ	Max	Units
V_{GS}	Gate Drive Voltage			6.5	V

(10) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

9. ESD Ratings

Symbol	Parameter	Max	Units
CDM	Charged Device Model (per JS-002-2014)	750	V

10. Thermal Resistance

Symbol	Parameter	Typ	Units
$R_{e\_JUNC-CASE}$	Junction-to-Case Thermal Resistance	0.55	°C/W

11. Electrical Characteristics

Conditions unless specified: V_{SS} = 400V, V_{GS} = 6.5V, T_{CASE} = 25°C, I_{SS} = 8.15A

Symbol	Parameter	Min	Typ	Max	Units	Conditions
4-Quadrant GaN Switch Characteristics						
I_{SSS}	Source-Source Leakage Current		70		µA	V_{SS} = 650V, V_{GS} = 0V
I_{SSS}	Source-Source Leakage Current		75		µA	V_{SS} = 650V, V_{GS} = 0V, T_{JUNC} = 150°C
I_{GSS}	Gate-Source Leakage Current		72		µA	V_{GS} = 6.5V
$R_{SS(ON)}$	Source-Source Resistance		80	110	mΩ	V_{GS} = 6.5V, I_{SS} = 8.15A
$R_{SS(ON)}$	Source-Source Resistance		192		mΩ	V_{GS} = 6.5V, I_{SS} = 8.15A, T_{JUNC} = 150°C (by Design)
$V_{GS1(th)}$	Gate Threshold Voltage	1	1.5	2.8	V	I_{S21} = 15.5mA, V_{S21} = 0.1V
$V_{S12\_Reverse}$	Source-Source Third Quadrant Conduction Voltage		3.3	5	V	V_{GS1} = 0V, V_{GS2} = 6.5V, I_{S12} = 8.15A
Q_{RR}	Reverse Recovery Charge		Zero		nC	
R_G	Internal Gate Resistance		400		mΩ	By Design
C_{ISS}	Input Capacitance		168		pF	V_{SS} = 400V, V_{GS} = 0V
C_{ISS1}	Input Capacitance		168		pF	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V
C_{OSS}	Output Capacitance		86		pF	V_{SS} = 400V, V_{GS} = 0V
C_{OSS1}	Output Capacitance		91		pF	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V
C_{RSS}	Reverse Transfer Capacitance		2		pF	V_{SS} = 400V, V_{GS} = 0V
C_{RSS1}	Reverse Transfer Capacitance		1.6		pF	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V
Q_G	Total Gate Charge for Each Gate		4.63		nC	V_{S21} = 400V, V_{GS1} = 0V to 6.5V, V_{GS2} = 0V
Q_{G1}	Total Gate Charge for Each Gate		5.29		nC	V_{S21} = 400V, V_{GS1} = 0V to 6.5V, V_{GS2} = 6.5V
Q_{GS}	Gate-Source Charge for Each Individual Gate		1.03		nC	V_{S21} = 400V, V_{GS1} = 0V to 6.5V, V_{GS2} = 0V
Q_{GS1}	Gate-Source Charge for Each Individual Gate		1.03		nC	V_{S21} = 400V, V_{GS1} = 0V to 6.5V, V_{GS2} = 6.5V

Q_{OSS}	Output Charge		50		nC	V_{SS} = 400V, V_{GS} = 0V
Q_{OSS1}	Output Charge		65		nC	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V
$C_{O(er)}$ (Note 10)	Effective Output Capacitance, Energy Related		105		pF	V_{SS} = 400V, V_{GS} = 0V
$C_{O(er)1}$ (Note 11)	Effective Output Capacitance, Energy Related		121		pF	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V
$C_{O(tr)}$ (Note 12)	Effective Output Capacitance, Time Related		124		pF	V_{SS} = 400V, V_{GS} = 0V
$C_{O(tr)1}$ (Note 13)	Effective Output Capacitance, Time Related		161		pF	V_{S21} = 400V, V_{GS1} = 0V, V_{GS2} = 6.5V

(10) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{SS} rises from 0V to 400V.

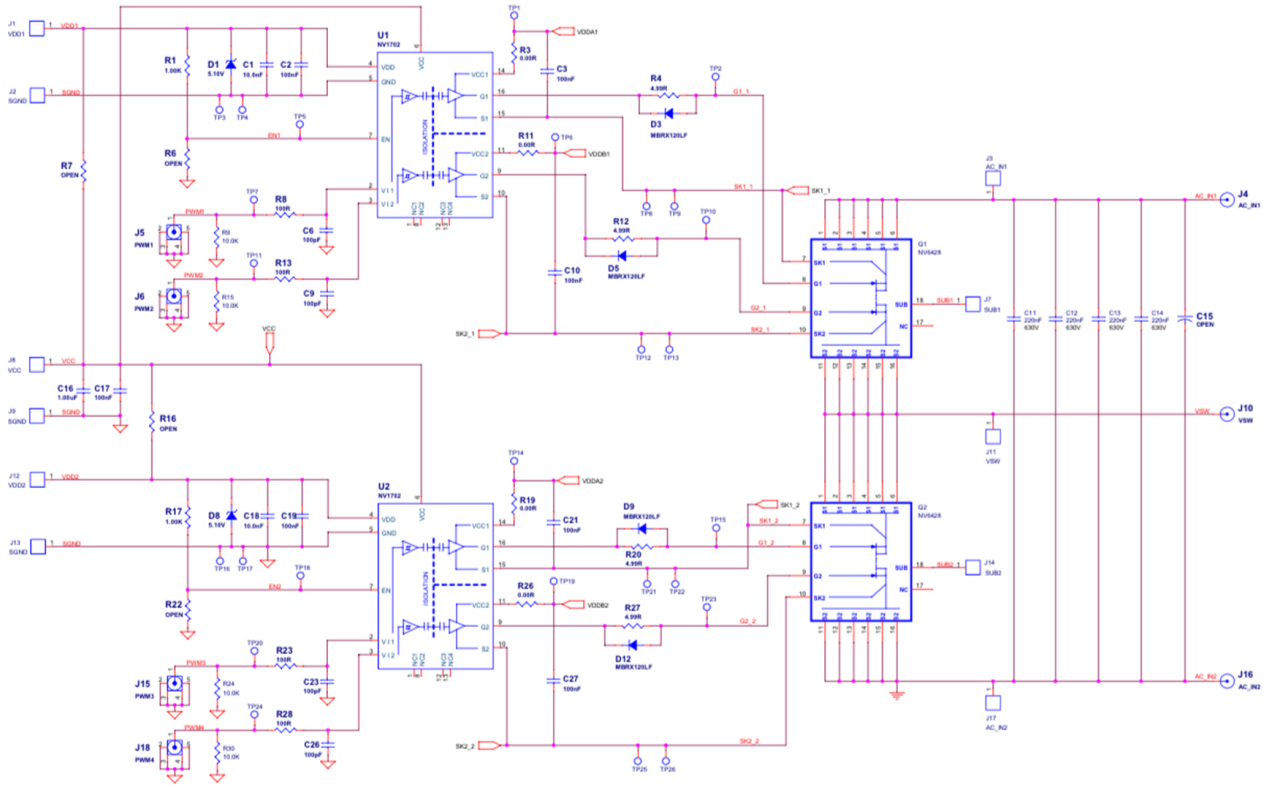
(11) $C_{O(er)1}$ is a fixed capacitance that gives the same stored energy as C_{OSS1} while V_{SS} rises from 0V to 400V.

(12) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{SS} rises from 0V to 400V.

(13) $C_{O(tr)1}$ is a fixed capacitance that gives the same charging time as C_{OSS1} while V_{SS} rises from 0V to 400V.

12. Inductive Switching Test Circuit

Schematic 1. Inductive Switching Test Circuit



13. Electrical Curves (GaN FET, T_{CASE} = 25°C unless otherwise specified)

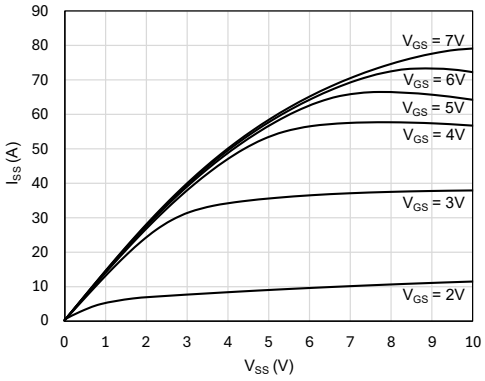


Fig. 1. I_{S21_PULSE} vs. V_{S21}, V_{GS2} = 6V, T_{JUNC} = 25°C

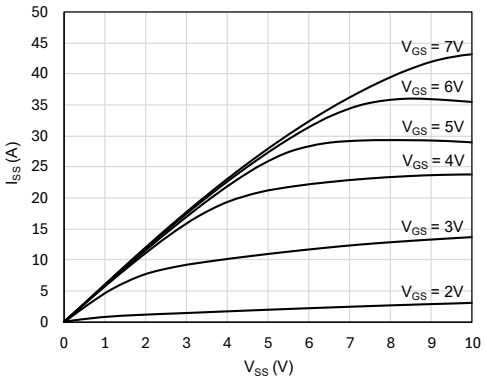


Fig. 2. I_{S21_PULSE} vs. V_{S21}, V_{GS2} = 6V, T_{JUNC} = 150°C

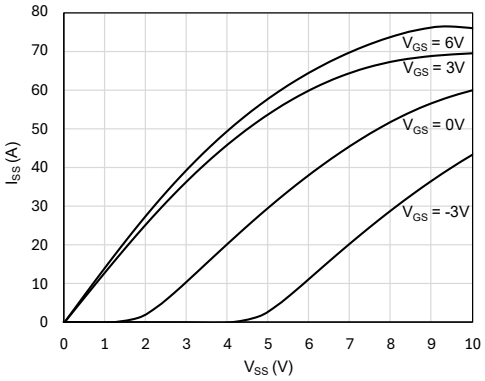


Fig. 3. Third Quadrant Conduction, V_{GS1} = 6V, T_{JUNC} = 25°C

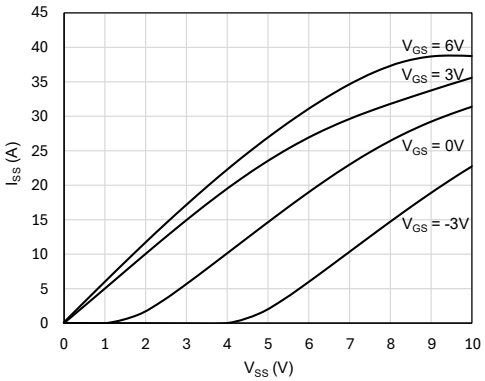


Fig. 4. Third Quadrant Conduction, V_{GS1} = 6V, T_{JUNC} = 150°C

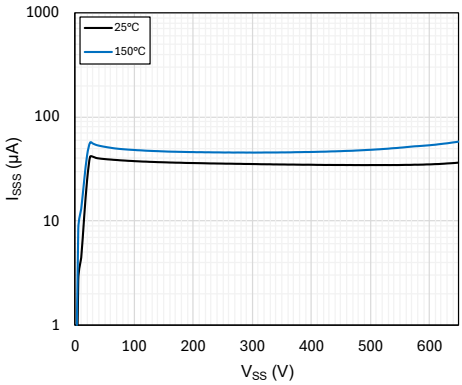


Fig. 5. I_{SSS} vs. V_{SS}, T_{JUNC} = 25°C, 150°C

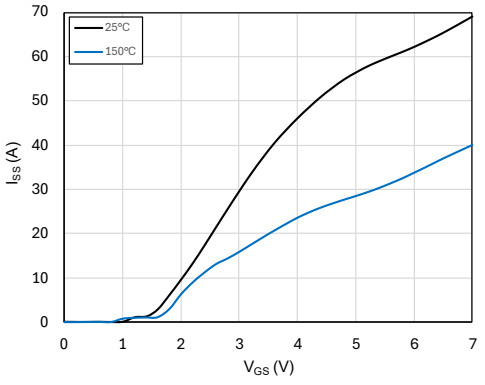


Fig. 6. I_{S21_PULSE} vs. V_{GS1}, V_{GS2} = 6V, V_{S21} = 10V

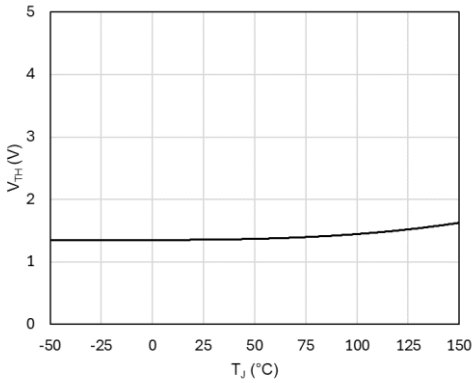


Fig. 7. $V_{GS(th)}$ vs. T_{JUNC}

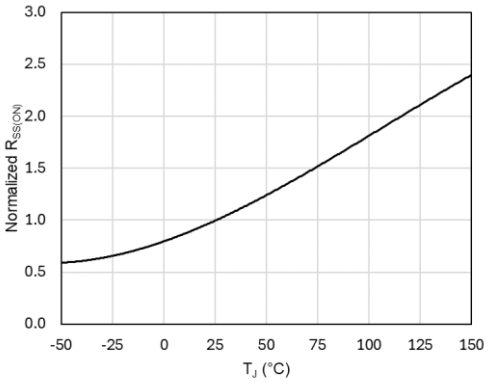


Fig. 8. Normalized $R_{SS\ (ON)}$ vs. T_{JUNC}

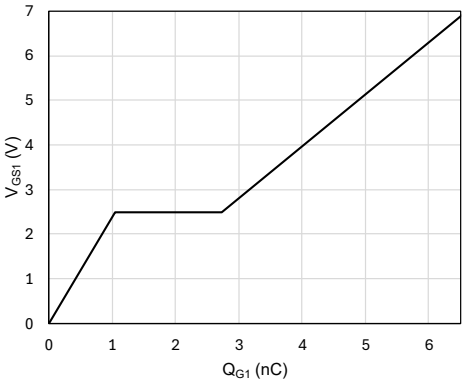


Fig. 9. V_{GS1} vs. Q_{G1}, V_{GS2} = 6V

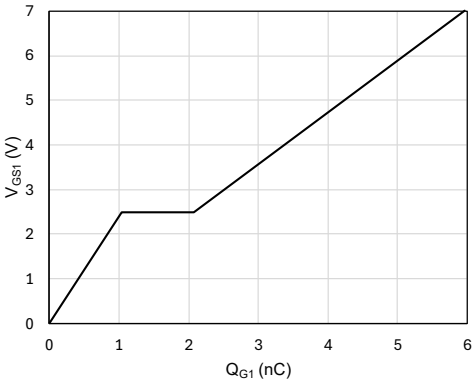


Fig. 10. V_{GS1} vs. Q_{G1}, V_{GS2} = 0V

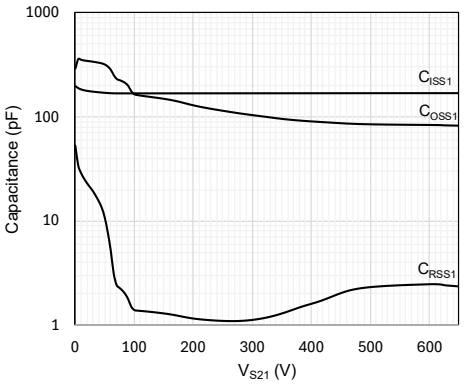


Fig. 11. C_{ISS1}, C_{OSS1}, C_{RSS1} vs. V_{S21}, V_{GS1} = 0V, V_{GS2} = 6V

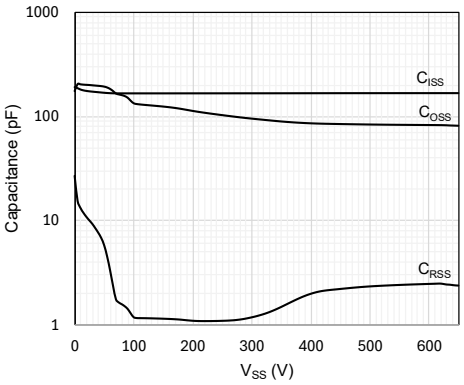


Fig. 12. C_{ISS}, C_{OSS}, C_{RSS} vs. V_{SS}, V_{GS} = 0V

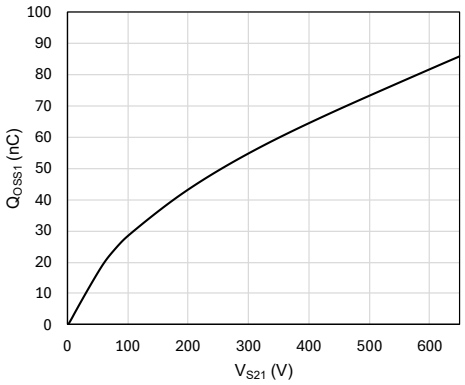


Fig. 13. Q_{OSS1} vs. V_{S21}, V_{GS1} = 0V, V_{GS2} = 6V

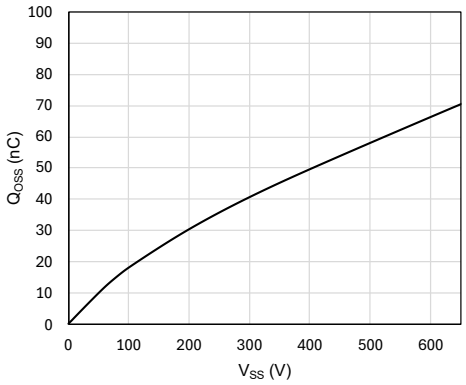


Fig. 14. Q_{OSS} vs. V_{SS}, V_{GS} = 0V

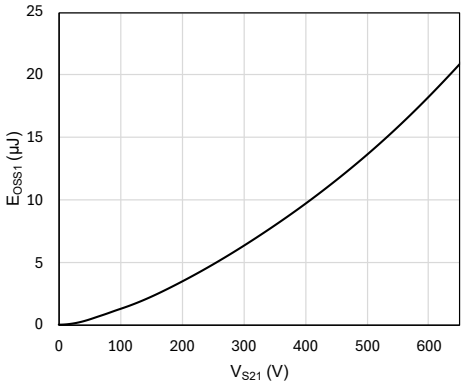


Fig. 15. E_{OSS1} vs. V_{S21}, V_{GS1} = 0V, V_{GS2} = 6V

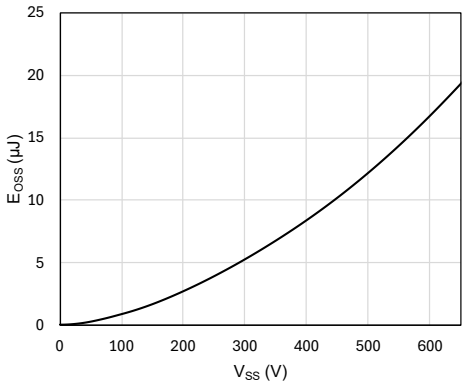


Fig. 16. E_{OSS} vs. V_{SS}, V_{GS} = 0V

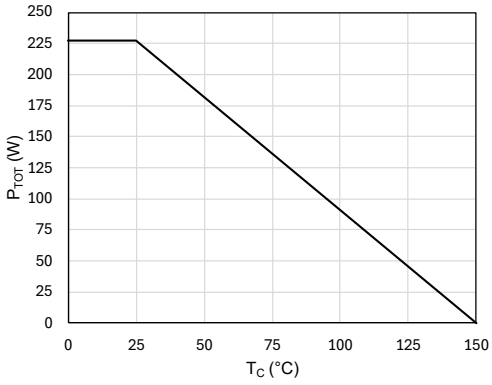


Fig. 17. $P_{DISSIPATION}$ vs. T_{CASE}

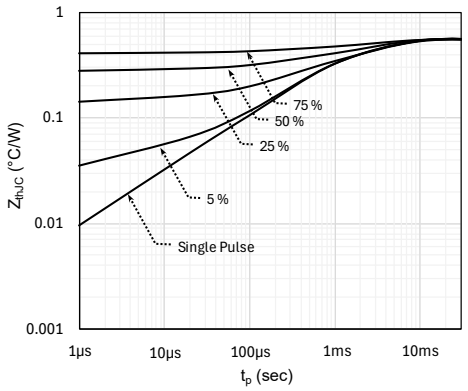


Fig. 18. Transient $R_{\Theta JUNC\text{-}CASE}$

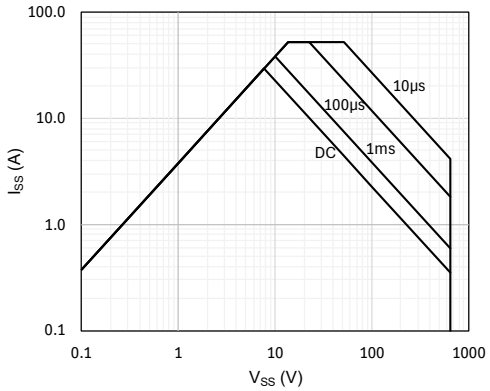
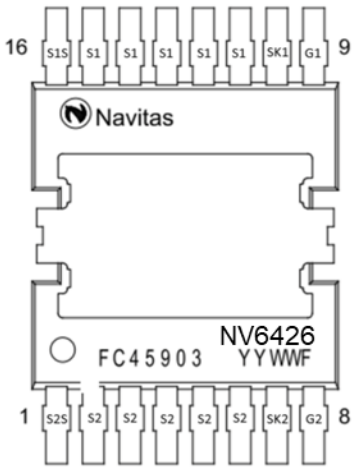


Fig. 19. Safe Operating Area, T_{JUNC} = 25°C

14. Pinout Table



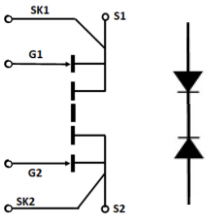
Pin		I/O	Description
Number	Symbol		
1	S2S	P	Connect to S2 on PCB
2-6	S2	P	Source 2 Terminal
7	SK2	G	Kelvin Source 2
8	G2	I	Gate 2
9	G1	I	Gate 1
10	SK1	G	Kelvin Source 1
11-15	S1	P	Source 1 Terminal
16	S1S	P	Connect to S1 on PCB
Top Pad	N/A	N/A	Substrate: Requires Isolation to Heatsink
Note: I = Input, P = Power, G = Ground			

15. Functional Description

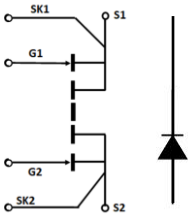
15.1. Operating Modes

NV6426 is a normally-off GaNFET device with two gates (G1, G2) and two sources (S1, S2). G1 acts with respect to S1, and G2 acts with respect to S2, but G2 does not act with respect to S1, and vice-versa. As a 4-Quadrant Switch (4QS), it is capable of blocking voltage in either or both directions, and conducting current in either or both directions, depending on the states of G1 and G2.

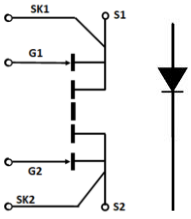
Mode 1 (V_{GS1} = 0V, V_{GS2} = 0V): Voltage is blocked in both the V_{S12} and V_{S21} direction. Current is blocked in both the I_{S12} and I_{S21} direction.



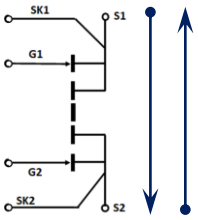
Mode 2 (V_{GS1} = 6.5V, V_{GS2} = 0V): Voltage is blocked in the V_{S12} direction only. Current flows in the I_{S21} direction but is blocked in the I_{S12} direction. V_{S21} should not exceed 7V.



Mode 3 (V_{GS1} = 0V, V_{GS2} = 6.5V): Voltage is blocked in the V_{S21} direction only. Current flows in the I_{S12} direction but is blocked in the I_{S21} direction. V_{S12} should not exceed 7V.



Mode 4 (V_{GS1} = 6.5V, V_{GS2} = 6.5V): Current can flow in either direction. If V_{S12} > V_{S21}, then current flows in the I_{S12} direction. If V_{S21} > V_{S12}, then current flows in the I_{S21} direction.



15.2. Integrated Substrate Clamp

NV6426 has a monolithic, integrated substrate clamping circuit which optimizes the silicon substrate potential under any bias condition applied between the two sources. This clamp circuit prevents undesired $R_{SS(ON)}$ increases that can happen when the silicon substrate potential is uncontrolled.

This major performance enhancement is possible by virtue of Navitas *GaNFast*™ technology and this functionality differentiates NV6426 from competitor parts.

15.3. Gate Driver and Gate Power Supply Selection

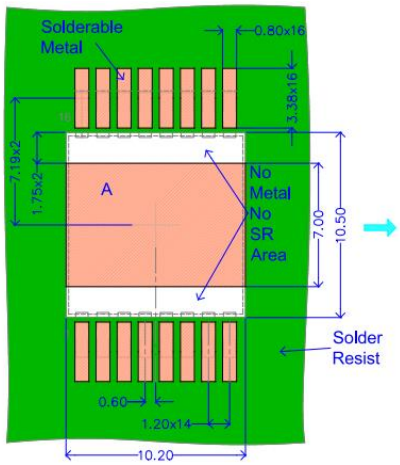
NV6426 Bi-Directional Switch requires two floating gate driver channels to provide PWM-generated gate drive inputs to the two gates. An isolated driver is recommended, providing 6V~6.5V output voltage for best performance and should be able to turn on both gate outputs simultaneously (Mode 4 operation). The type of isolation is dependent on the circuit and system requirements. Functional isolation may be enough in many cases, but in some cases safety isolation may also be needed.

At least one of the two gates will not be referenced to ground or a DC rail and will require a drive channel that can float to high voltage that matches the range of the source it is driving. In some applications, both sources are switching nodes, so both gate drive outputs and the power supplies for them must be able to float to remain referenced to the source being driven. In some circuits, a ground referenced power supply and a bootstrap power supply is sufficient, while in others an isolated floating power supply for one or both gate drives may be required.

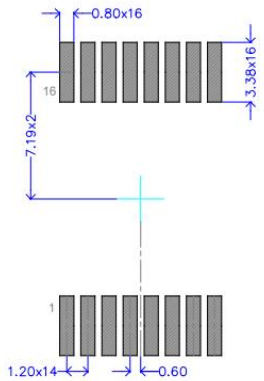
15.4. PCB Layout Guidelines and PCBA SMT Guidelines

PCB layout is critical for thermal management, noise immunity, and proper operation of the device. The following rules should be followed carefully during the design of the PCB layout:

- Do not run power SOURCE current through SK pin!



RECOMMENDED PCB FOOTPRINT

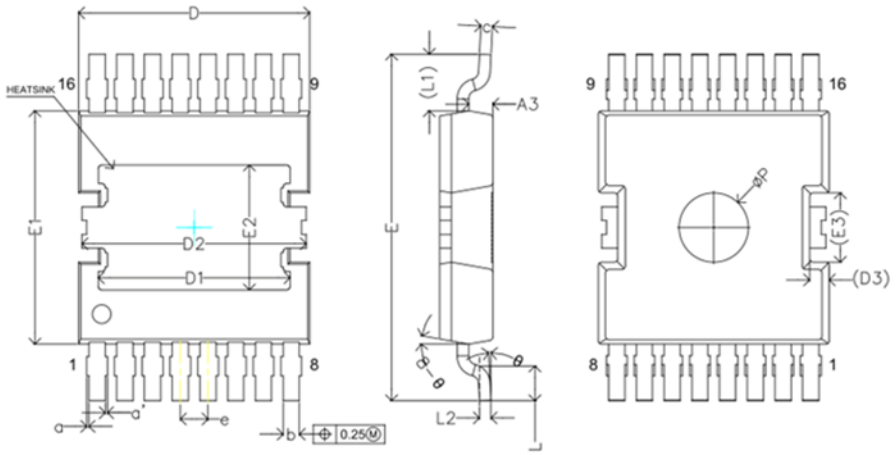


RECOMMENDED STENCIL OPENING

PCBA SMT Guidelines:

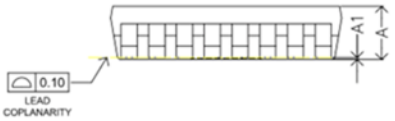
- 1.6mm thick FR4, 4-Layer 2-Oz Cu
- Solder Mask per DWG on left
- Solder Stencil per Customer's PCBA SMT
- Solder Reflow Profile per PCBA SMT Vendor
- Recommended Solder Paste: SAC305
- Recommended 10% ***maximum*** Voids

16. Package Outline Dimensions:



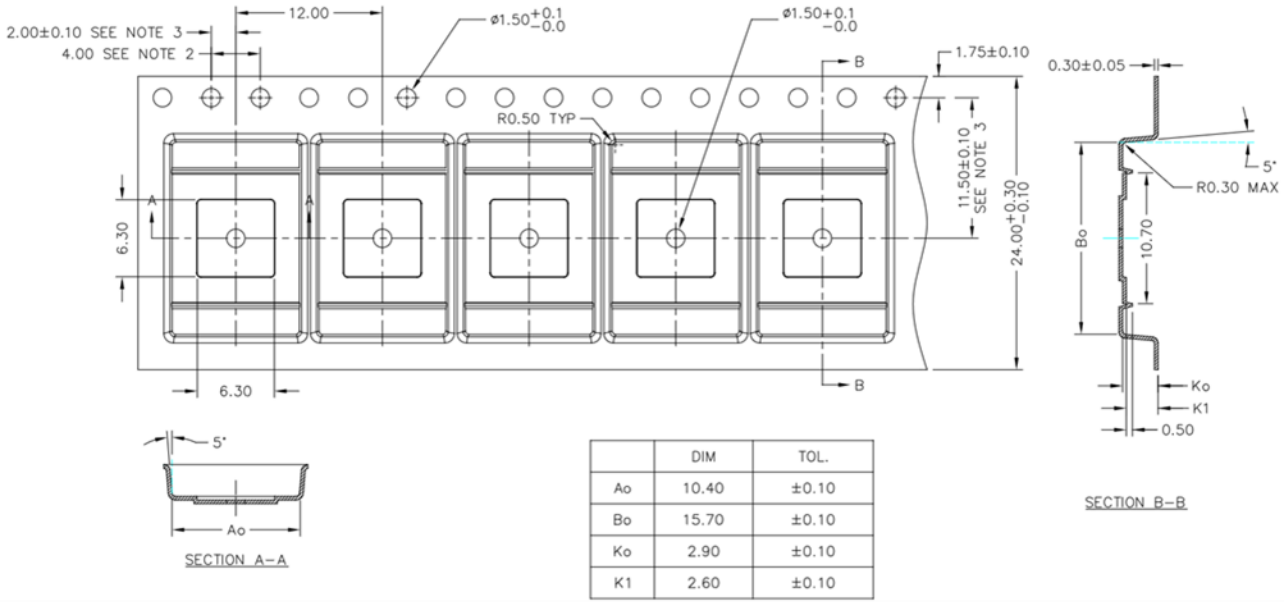
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.25	2.30	2.35
A1	0.01	0.08	0.16
A3	0.99	1.04	1.09
a	0.00	--	0.15
a'	0.00	--	0.15
b	0.60	0.70	0.80
c	0.40	0.50	0.60
D	9.70	10.00	10.10
D1	8.20	8.30	8.40
D2	9.50	9.70	9.90
D3		0.85REF	
E	14.80	15.00	15.20
E1	10.00	10.10	10.30
E2	5.30	5.40	5.50
E3		3.00REF	
e	1.10	1.20	1.30
L	1.40	1.50	1.60
L1		2.45REF	
L2		0.50BSC	
øP	2.90	3.00	3.10
θ	0°	--	8°
θ1	8°	10°	12°

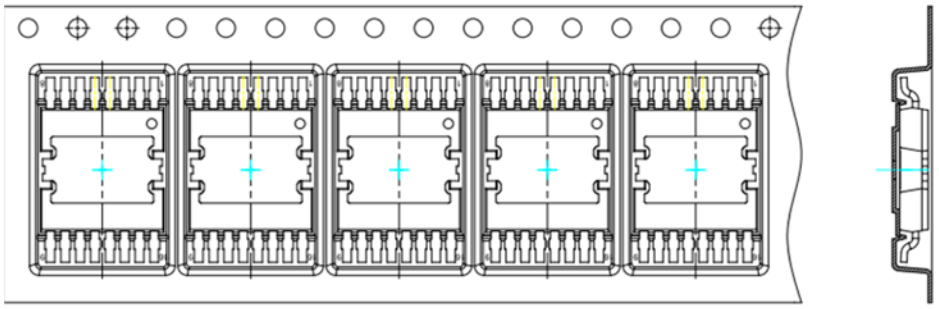


NOTES:
1.ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

17. TnR Drawing



	DIM	TOL.
Ao	10.40	±0.10
Bo	15.70	±0.10
Ko	2.90	±0.10
K1	2.60	±0.10



18. Ordering Information

Part Number	Qualification	Package	MSL Rating	TnR Dia. and Qty
NV6426	JEDEC	TOLT-16L Top-cooled SMD	3	Standard (13” dia) Qty1,500
NV6426-RA				Mini-Reel (7” dia) Qty450

19. Revision History

Date	Status	Notes
June 3rd, 2025	Preliminary	• Updated Electrical Characteristics and Curves data
July 7th, 2025	Final	• Updated Electrical Characteristics and Curves data

Additional Information

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